REMARKS

With the foregoing amendments to the specification, Applicants amend the related applications section to include the U.S. patent application numbers of concurrently filed, related applications.

In response to the Office Action mailed August 4, 2006[1], Applicants respectfully request reconsideration. Claims 1-46 are pending in the application of which claims 1, 31, and 32 are independent.

Applicants gratefully appreciate the Examiner's indication of allowable subject matter in claims 12-30 and 39-45.

Double Patenting Rejection

In the Office Action mailed August 4, 2006, the Examiner rejected claims 1-46 under the judicially created doctrine of obviousness-type double patenting over claims 1-30 of copending Application No. 10/787,320 (hereinafter "'320"), claims 1-25 of copending Application No. 10/787,321 (hereinafter "'321"), claims 1-60 of copending Application No. 10/787,322 (hereinafter "'322"), and claims 1-37 of copending Application No. 10/787,324 (hereinafter "'324").

While Applicants respectfully disagree with the provisional obviousness-type double patenting rejections, filed herewith is a terminal disclaimer in compliance with 37 CFR 1.321, which overcomes the provisional obviousness-type double patenting rejection of claims 1-46 over claims 1-37 of copending Application No. '324 and claims 1-60 of copending Application No. '322.

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[1] The Office Action may contain statements characterizing the related art, case law, and claims. Regardless of whether any such statements are specifically identified herein, Applicants decline to automatically subscribe to any statements in the Office Action.

Applicants contend that a terminal disclaimer is particularly not necessary for overcoming the provisional double patenting rejection with respect to claims 1-30 of '320 and claims 1-25 of '321 where these claims are clearly patentably distinct from claims 1-46 of the instant application.

Claims 1-30 of '320 and claims 1-25 of '321 do not disclose or suggest every element of claims 1-46. For example, claims 1-30 of '320 and claims 1-25 of '321 do not disclose or suggest two virtualization layers as described in independent claims 1 and 32 of the instant application. Similarly, independent claim 31 of the instant application is directed to a multi-tier switching system comprising: "first tier storage processors..." and "second tier storage processors...." These elements are non-obvious in view of in Claims 1-30 of '320 or claims 1-25 of '321.

In view of the foregoing arguments, Applicants respectfully request withdrawal of the provisional double patenting rejection over claims 1-30 of copending Application No. 10/787,320 and claims 1-25 of copending Application No. 10/787,321.

Rejections Under 35 U.S.C. § 102

In the Office Action mailed August 4, 2006, the Examiner rejected claims 1-11, 31, 32-38, and 46 under 35 U.S.C. §102(e) as being anticipated by Varagur Chandrasekaran (U.S. Patent No. 6,948,044), hereinafter "Chandrasekaran". These rejections should be withdrawn because Applicants' claims patentably distinguish over Chandrasekaran.

To properly establish that a prior art reference anticipates a claimed invention under 35 U.S.C. § 102, each and every element of the claims in issue must be found, either expressly described or under principles of inherency, in the single prior art

reference. Nowhere does Chandrasekaran disclose "a first virtualization layer that maintains first tier objects..." and "a second virtualization layer that maintains second tier objects..." as recited in independent claims 1, 31, and 32.

The Examiner cites Chandrasekaran Col 5, lines 1-67 as disclosing the above-mentioned elements. However, in this reference, Chandrasekaran discloses a method using a single virtualization layer for determining the physical location for a data block to be written. Chandrasekaran discloses a single object, a linked list, which contains information about the size of the physical partition, offset from the start of the virtual disk, the location of the physical partition, and the actual start address in the physical disk. (Chandrasekaran Col 5, lines 57-64). Neither in the referenced location nor elsewhere in the patent does Chandrasekaran disclose or suggest that information reflecting a relationship between the physical block addresses and one or more logical partitions of virtual volume data and information reflecting the logical configuration of the virtual volume should be in separate virtualization layers containing separate tiered objects. The single-layer, single-tiered architecture of Chandrasekaran and the multi-layer, multi-tiered architecture in the instant application are patentably distinct architectures.

Since Chandrasekaran does not disclose or suggest "a second virtualization layer that maintains a second tier object including information reflecting a logical configuration of the virtual volume", the rejection under 35 U.S.C. § 102 of claim 1 as well as the rejection of claims 31 and 32 which contain similar elements, should be withdrawn. In addition, dependent claims 2-30, and 33-46 are allowable under 35 U.S.C. § 102 at least since they depend from claims 1 and 32.

In view of the foregoing amendments to claims and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: November 3, 2006

By: _____
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